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Remarks

Attached, as an Appendix, is a marked up reproduction of the changes made to the claims by the current amendments. Additions have been underscored and deletions have been stricken. In particular, claims 1, 3, 6,12, and 45 have been amended. Therefore, claims 1-14, and 45-46 are pending in the application.

Objection to Claims 1, 3, 6, 12 and 45

Claims 1, 3, 6, 12, and 45 are objected to for the noted informalities in the official action. The objected claims are accordingly amended by the above claim amendments, which are unrelated to patentability issues.

Claim Rejections - 35 USC § 102(b)/103(a)

Claims 1, 3, 5-9, 11 and 45 are rejected under 35 USC 102(b) as being anticipated by, or in the alternative, under 35 USC 103(a) as obvious over Pan (US 5,750,435). Claims 2, 4, 12-14 and 46 are rejected as being unpatentable over Pan. Claim 10 is rejected as being unpatentable over Pan in view of Admitted Prior Art (APA). Claims 12-14 are rejected as being unpatentable over Pan in view of Motoyoshi et al (JP 6-53492).

As previously pointed out by the Applicants, Pan teaches that providing hardening ions 18 into the gate oxide 14 beneath both edges of the gate electrode 16 is critical to his invention. Pan also discloses providing hardening ions to the exposed surfaces of the gate electrode16, the exposed surfaces of the gate oxide, and the upper surface of the semiconductor substrate 10. See column 5, line 60 - column 6, line 5. Therefore, except for the unhardened portion of the gate oxide directly underneath and inwards of both gate electrode edges, the ion concentration in the remaining hardened portions of the oxide is substantially the same. Accordingly, Pan does not teach or suggest a circuit structure having an overlap region of the oxide layer located beneath the gate structure and adjacent a first leading edge of the gate structure and inward of a second leading edge of the gate structure, which has a predetermined ion implant concentration higher than in remaining oxide layer portions adjacent both sides of the overlap region, as is recited by amended independent claim 1. Pan further does not teach or suggest a circuit structure having a portion of a gate oxide layer which defines an overlap region, which is beneath a gate electrode

inward of a source region and adjacent a drain region, and which has an ion implant concentration higher than in remaining portions of the oxide layer adjacent both sides of the overlap region, as is recited by amended independent claims 3, 12, and 45.

Motoyoshi et al. discloses uniform orthogonal fluorine implanting over the entire surface of gate oxide. Accordingly, Motoyoshi et al. fail to correct the above noted deficiency of Pan. Accordingly, one skilled in the art combining the teachings of Motoyoshi et al. with Pan would fail to produce the claimed invention recited in amended independent claim 12.

The remaining rejections are noted by the Applicants but are believed moot in view of the above amendments to independent claims 1, 3, 12, and 45. Accordingly, Applicants assert that claims 1,3, 12 and 45, and the claims that depend therefrom, are patentable over the cited prior art and, therefore, respectfully requests that the anticipation and obviousness rejections to the claims be withdrawn.

CONCLUSION

The Applicants respectfully submit that, in view of the above amendments and remarks, the application is now in condition for allowance. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,

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Appendix

Version indicating changes made, additions underscored, deletions stricken.

In the claims

1. (Currently Amended) A circuit structure comprising:

a semiconductor layer;

an oxide layer formed on said semiconductor layer;

a gate structure formed on said oxide layer having ~~a defined~~ first and second leading edges; and

an overlap region of the oxide layer located beneath said gate structure and adjacent said first leading edge and inward of said second leading edge, said overlap region having a predetermined ion implant concentration higher than in remaining ~~adjacent~~ oxide layer portions adjacent both sides of said overlap region, said predetermined implant concentration being sufficient to increase the electrical gate oxide thickness in said overlap region.

3. (Currently Amended) A circuit structure comprising:

a semiconductor layer;

a source region and a drain region in said semiconductor layer which are lightly doped with a first conductivity-type dopant;

a channel region located between said source/drain regions;

a gate oxide layer located on a surface of said channel region; and

a gate electrode located on said gate oxide layer, wherein a portion of said gate oxide layer defines an overlap region, which is beneath said gate electrode inward of said source region and adjacent said drain region ~~and which defines an overlap region~~, said overlap region having an ion implant concentration higher than in remaining portions of said oxide layer adjacent both sides of the overlap region, which is effective to lower the surface electrical field in said overlap region.

6. (Currently Amended) The circuit structure according to claim 3, further including a pair of spacers adjacent said gate electrode.

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12. (Currently Amended) A circuit structure comprising:

a semiconductor layer;

a first dopant-type MOS transistor is situated on said semiconductor layer having:

a source region and a drain region in said semiconductor layer which are doped with a first conductivity-type dopant;

a channel region located between said source/drain regions;

a gate oxide layer located on a surface of said channel region; and

a gate electrode located on said gate oxide layer, wherein a portion of said gate oxide layer defines an overlap region, which is beneath said gate electrode inward of said source region and adjacent said drain region ~~and which defines an overlap region~~, said overlap region having an ion implant concentration higher than in remaining portions of said gate oxide layer adjacent both sides of the overlap region, which is effective to lower the surface electrical field in said overlap region; and,

a second-type dopant MOS transistor which is complementary to said first dopant-type MOS transistor, said second-type dopant MOS transistor is situated on said semiconductor layer and includes a second gate oxide layer, two complementary source/drain regions which are doped with a second conductivity-type dopant, and a complementary gate electrode located on said second gate oxide layer.

45. (Currently Amended) A circuit structure comprising:

a semiconductor layer having a source region, a drain region, and a channel region located between said source/drain regions;

a gate oxide layer located at least on a surface of said channel region; and

a gate electrode located on said gate oxide layer, wherein a first portion of said gate oxide layer beneath said gate electrode and adjacent said drain region has a higher ion implant concentration than in remaining portions of said gate oxide layer adjacent both sides of said first portion.